REPLACEMENT SHEET

ATTY DKT. NO.: U.S. SERIAL NO.: 10/720,730 NOVEMBER 24, 2

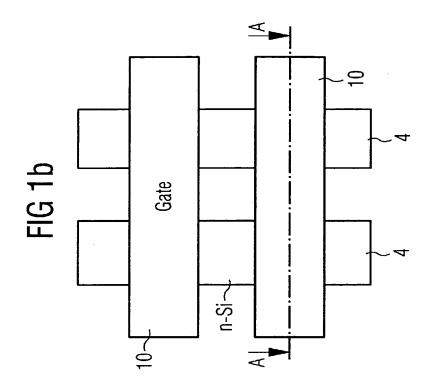
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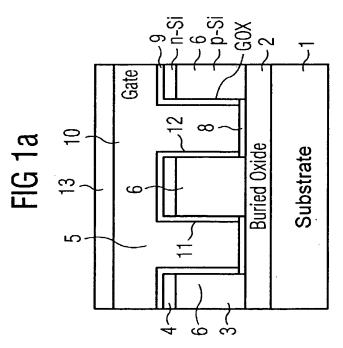
TITLE: INVENTOR(S): NOVEMBER 24, 2003
DRAM CELL ARRANGEMENT WITH VERTICAL MOS
TRANSISTORS, AND METHOD FOR ITS FABRICATION
TILL SCHLÖSSER ET AL.
SHEET 1 OF:

SHEET 1 OF 3

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REPLACEMENT SHEET

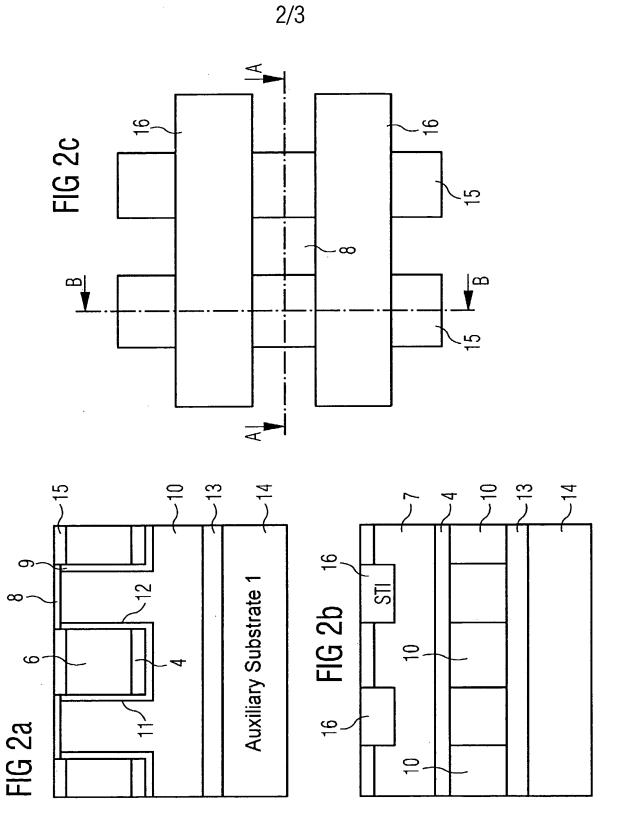
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INFN/WB0037 10/720,730

CONF. NO.: 2757

NOVEMBER 24, 2003
DRAM CELL ARRANGEMENT WITH VERTICAL MOS
TRANSISTORS, AND METHOD FOR ITS FABRICATION TILL SCHLÖSSER ET AL. SHEET 2 OF 3

INVENTOR(S):



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INFN/WB0037 10/720,730 NOVEMBER 24, 2003

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INVENTOR(S):

DRAM CELL ARRANGEMENT WITH VERTICAL MOS TRANSISTORS, AND METHOD FOR ITS FABRICATION TILL SCHLÖSSER ET AL. SHEET 3 OF 3

3/3

